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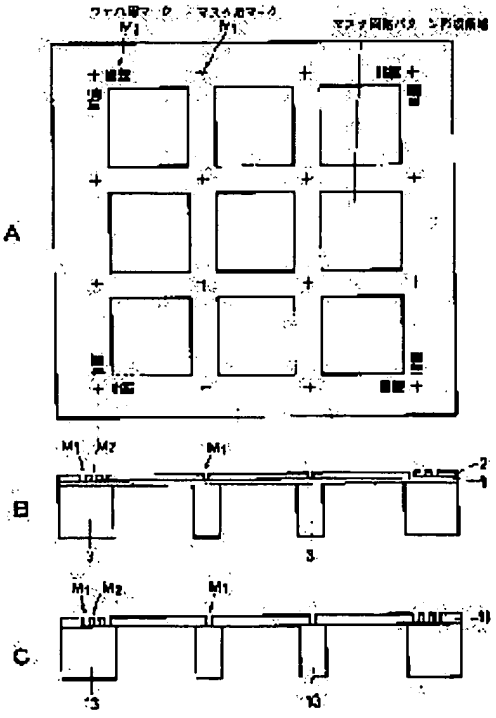
(54) MEMBER FOR PREPARING MASK AND METHOD FOR PREPARING THE SAME, MASK AND METHOD FOR PREPARING THE SAME, EXPOSURE METHOD AND METHOD FOR PREPARING SEMICONDUCTOR DEVICE

(57)Abstract:

PROBLEM TO BE SOLVED: To expose with high precision a substrate with a mask by preparing the mask for contraction, division, transfer and exposure of charged particle beams at a low cost and with high precision.

SOLUTION: In a support area of a mask blank consisting of a plurality of areas, where a mask circuit pattern is formed and a supporting area where a plurality of these areas are separated and held, two kinds of positioning marks M1 and M2 are formed to expose a mask circuit pattern with the mark M1 as reference and to expose a substrate with the mark M2 as reference.



* NOTICES *

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention]Especially this invention is applied to exposure of substrates, such as a wafer by a charged particle beam, for example, an electron beam, about a member for mask production, a manufacturing method for the same, a mask, a manufacturing method for the same, an exposure method, and the manufacturing method of a semiconductor device, and is preferred.
[0002]
[Description of the Prior Art]A semiconductor integrated circuit device, a liquid crystal display, a CCD device, etc. are manufactured using the ultra-fine processing technology of a semiconductor. In order to form the pattern which continues carrying out minuteness making with high integration of these semiconductor devices, exposure by the charged particle beam, especially an electron beam attracts attention. However, although an electron-beam-lithography method is excellent in minuteness making, it has the fault that a throughput (throughput per unit time) is low. The variable molding exposure method which deflects an electron beam between the molded masks of two sheets, and makes the electron beam shape of a desired size in about a maximum of 5 micrometers in order to raise this throughput, A circuit pattern part is made to the molded mask of the lower berth, the partial one-shot exposure method which exposes two or more figure patterns at an electron beam shot once is devised, and the electron-beam-lithography machine which combined both is already put in practical use. however, in exposure of the circuit pattern which recent years integrated highly, a throughput is markedly alike also by this partial one-shot exposure method compared with the exposure system using the light which is the present mainstream, and it is low.
[0003]In order to solve the problem of the throughput in this electron-beam-lithography method, The mask provided with the circuit pattern of the whole integrated circuit chip of a

piece is irradiated with an electron beam, and the electron beam reduction transfer device which carries out reduction transfer (reduction percentage is 1/4) of the image of the pattern of the irradiation area with a projection lens is devised (for example, JP,5-160012,A). In this electron beam reduction transfer exposure method, to the mask total range equivalent to the whole integrated circuit chip of a piece, if it is going to carry out the package exposure of the electron beam, it cannot expose with sufficient accuracy. Then, so that the view of an electron optics system and the pattern on a mask may be divided into two or more fields, the divided pattern may be connected on a wafer and it may become a circuit pattern of the whole integrated circuit chip of a piece correctly, The electron beam reduction division transfer exposure method exposed one by one is devised (for example, JP,5-251317,A).

[0004]Although high resolution nature and a high throughput can be obtained by using this electron beam reduction division transfer exposure method, for that purpose, high degree of accuracy and a high resolution mask are needed. The reduction percentage of reduction percentage is the same as that of the mask of the exposure machine which used light almost in one fourth of masks. Supposing the same performance as the mask exposure machine for lights is called for, a very expensive mask exposure machine is needed. In order to attain highly precise exposure all over a mask, while exposing various amendments, it is needed, and a throughput becomes low.

[0005]In order to attain high accuracy of position, in JP,11-38599,A, the position detecting mark is formed all over the mask substrate, and when exposing a circuit pattern on a mask substrate, the method of obtaining a highly precise mask by using the position detecting mark and performing position amendment is proposed. However, in this method, there are problems that neither a throughput's being low nor the pattern formation device excellent in long dimension accuracy is obtained at present, like there is nothing.

[0006]Although the exposure machine is designed in the electron beam reduction division transfer exposure method transfer on a substrate the circuit pattern formed on the mask as correctly as possible, there is a danger that it will still assemble and a delicate gap will occur in transfer with each exposure machine in the accuracy at the time, etc. Although such a gap can be then amended according to the device status at that time in electron beam straight-writing exposure machines, such as a variable molding exposure method and a partial one-shot exposure method, since the circuit pattern on a mask is collectively transferred by a transfer exposure method, amendment of such an electron optics system is difficult.

[0007]

[Problem(s) to be Solved by the Invention]An object of this invention is to solve at once the above-mentioned technical problem which conventional technology has. Namely, this Object of the Invention, The mask for charged particle beam reduction division transfer exposure. It is in providing a member for mask production which can be manufactured with high precision by

low cost, a manufacturing method for the same, a mask, a manufacturing method for the same, the exposure method using such a mask, and the manufacturing method of the semiconductor device using such a mask.

[0008]

[Means for Solving the Problem]As a result of inquiring wholeheartedly, in order to solve many above-mentioned technical problems which conventional technology has, this invention person finds out that the following policy is effective, and used to come to think out this invention.

[0009]1. Form an alignment mark for mask exposure, and an alignment mark for substrate exposure of a wafer etc. in a member for mask production (mask blank) before exposing a mask circuit pattern, and expose a mask circuit pattern, referring to the alignment mark for mask exposure. 2. Division transfer exposure is performed using a test mask for accuracy-of-position measurement, from a transferred patterns circuit for accuracy-of-position detection, a gap of an electron optics system of an electron beam reduction division transfer exposure machine and a stage mechanism system and distortion are detected, and the gap and distortion are amended at the time of mask circuit pattern exposure.

[0010]Namely, in order that this invention may solve an aforementioned problem, an invention of the 1st of this invention, A member for mask production which consists of two or more fields in which a mask circuit pattern is formed, and a support region which separates and holds two or more of these fields, and in which a mask circuit pattern is not formed is characterized by comprising:

The 1st alignment mark used at the time of exposure for forming a mask circuit pattern in the above-mentioned support region.

The 2nd alignment mark used at the time of exposure of an exposure substrate.

[0011]Two or more fields in which a mask circuit pattern is formed as for the 2nd invention of this invention, The 1st alignment mark used at the time of exposure for consisting of a support region in which a mask circuit pattern is not formed, and forming a mask circuit pattern in the above-mentioned support region which separates and holds two or more of these fields, It is a manufacturing method of a member for mask production which has the 2nd alignment mark used at the time of exposure of an exposure substrate, all the 1st alignment mark of the above and 2nd alignment mark of the above on a member for mask production are put in block, and it was made to form.

[0012]Two or more fields in which a mask circuit pattern is formed as for the 3rd invention of this invention, The 1st alignment mark used at the time of exposure for consisting of a support region in which a mask circuit pattern is not formed, and forming a mask circuit pattern in the above-mentioned support region which separates and holds two or more of these fields, It is a manufacturing method of a member for mask production which has the 2nd alignment mark

used at the time of exposure of an exposure substrate, All the 1st alignment mark of the above and 2nd alignment mark of the above which are formed on a member for mask production are divided into two or more groups containing two or more 1st alignment mark of the above and 2nd alignment mark of the above, The 1st alignment mark of the above and the 2nd alignment mark of the above were formed by exposing one by one for every group of two or more of these groups.

[0013]Mask of this invention which consists of two or more fields in which a mask circuit pattern was formed, and a support region in which a mask circuit pattern which separates and holds two or more of these fields is not formed is characterized by that the 4th invention of this invention comprises the following.

The 1st alignment mark used at the time of exposure for forming a mask circuit pattern in the above-mentioned support region.

The 2nd alignment mark used at the time of exposure of an exposure substrate.

[0014]Two or more fields in which a mask circuit pattern was formed as for the 5th invention of this invention, The 1st alignment mark used at the time of exposure for consisting of a support region in which a mask circuit pattern is not formed, and forming a mask circuit pattern in the above-mentioned support region which separates and holds two or more of these fields, It is a manufacturing method of a mask which has the 2nd alignment mark used at the time of exposure of an exposure substrate, all the 1st alignment mark of the above and 2nd alignment mark of the above on a member for mask production are put in block, and it was made to form.

[0015]Two or more fields in which a mask circuit pattern was formed as for the 6th invention of this invention, The 1st alignment mark used at the time of exposure for consisting of a support region in which a mask circuit pattern is not formed, and forming a mask circuit pattern in the above-mentioned support region which separates and holds two or more of these fields, It is a manufacturing method of a mask which has the 2nd alignment mark used at the time of exposure of an exposure substrate, All the 1st alignment mark of the above and 2nd alignment mark of the above which are formed on a member for mask production are divided into two or more groups containing two or more 1st alignment mark of the above and 2nd alignment mark of the above, The 1st alignment mark of the above and the 2nd alignment mark of the above were formed by exposing one by one for every group of two or more of these groups.

[0016]Two or more relative distances between groups are suitably found here by measuring a relative distance of two or more 1st alignment marks between groups and the 2nd alignment mark, Correction is added according to the result and exposure by a charged particle beam for forming a mask circuit pattern in two or more fields using the 1st alignment mark is performed.

[0017]Two or more fields in which a mask circuit pattern was formed as for the 7th invention of

this invention, The 1st alignment mark used at the time of exposure for consisting of a support region in which a mask circuit pattern is not formed, and forming a mask circuit pattern in the above-mentioned support region which separates and holds two or more of these fields, It is a manufacturing method of a mask used for having the 2nd alignment mark used at the time of exposure of an exposure substrate, and exposing an exposure substrate with a charged particle beam reduction division transfer exposure device using the 2nd alignment mark of the above, Reduction division transfer of the above-mentioned position gap measured pattern is carried out at the above-mentioned exposure substrate by exposing an exposure substrate using a test mask which has a position gap measured pattern with the above-mentioned charged particle beam reduction division transfer exposure device, The above-mentioned exposure substrate is asked for the amount of position gaps and a position gap correction amount at the time of exposure of the above-mentioned charged particle beam reduction division transfer exposure device using the above-mentioned position gap measured pattern by which reduction division transfer was carried out, A mask which amended the above-mentioned mask was produced by performing exposure for adding correction by the above-mentioned position gap correction amount, and forming the above-mentioned mask circuit pattern so that the above-mentioned amount of position gaps may be amended.

[0018]Two or more fields in which a mask circuit pattern was formed as for the 8th invention of this invention, The 1st alignment mark used at the time of exposure for consisting of a support region in which a mask circuit pattern is not formed, and forming a mask circuit pattern in the above-mentioned support region which separates and holds two or more of these fields, It was made to perform exposure by a charged particle beam to an exposure substrate using the 2nd alignment mark of the above using a mask which has the 2nd alignment mark used at the time of exposure of an exposure substrate.

[0019]Two or more fields in which a mask circuit pattern was formed as for the 9th invention of this invention, The 1st alignment mark used at the time of exposure for consisting of a support region in which a mask circuit pattern is not formed, and forming a mask circuit pattern in the above-mentioned support region which separates and holds two or more of these fields, A mask which has the 2nd alignment mark used at the time of exposure of an exposure substrate is used, It is the exposure method which was made to expose an exposure substrate with a charged particle beam reduction division transfer exposure device using the 2nd alignment mark of the above, Reduction division transfer of the above-mentioned position gap measured pattern is carried out at the above-mentioned exposure substrate by exposing an exposure substrate using a test mask which has a position gap measured pattern with the above-mentioned charged particle beam reduction division transfer exposure device, The above-mentioned exposure substrate is asked for the amount of position gaps and a position gap correction amount at the time of exposure of the above-mentioned charged particle beam

reduction division transfer exposure device using the above-mentioned position gap measured pattern by which reduction division transfer was carried out, A mask which amended the above-mentioned mask by performing exposure for adding correction by the above-mentioned position gap correction amount, and forming the above-mentioned mask circuit pattern so that the above-mentioned amount of position gaps may be amended is produced, It was made to expose to an exposure substrate with the above-mentioned charged particle beam reduction division transfer exposure device using this mask.

[0020]When using two or more charged particle beam reduction division transfer exposure devices for exposure of substrates, such as a wafer, especially, exposing in the following procedures is preferred. That is, reduction division transfer of the position gap measured pattern is carried out at an exposure substrate by exposing an exposure substrate first using the same test mask with two or more charged particle beam reduction division transfer exposure devices. Next, an exposure substrate is asked for the amount of position gaps and a position gap correction amount at the time of each exposure of two or more charged particle beam reduction division transfer exposure devices using a position gap measured pattern by which reduction division transfer was carried out. Next, a mask which amended the above-mentioned mask is produced to each of two or more above charged particle beam reduction division transfer exposure devices by performing exposure for adding correction by a position gap correction amount, and forming a mask circuit pattern so that this amount of position gaps may be amended. And it exposes to an exposure substrate using these masks by each of two or more above charged particle beam reduction division transfer exposure devices.

[0021]Two or more fields in which a mask circuit pattern was formed as for the 10th invention of this invention, The 1st alignment mark used at the time of exposure for consisting of a support region in which a mask circuit pattern is not formed, and forming a mask circuit pattern in the above-mentioned support region which separates and holds two or more of these fields, In a manufacturing method of a semiconductor device which has two or more exposure processes exposed to a semiconductor substrate with a charged particle beam reduction division transfer exposure device using a mask which has the 2nd alignment mark used at the time of exposure of an exposure substrate, The same mask was used as a mask for exposure for forming the 1st alignment mark of the above and the 2nd alignment mark of the above in two or more above-mentioned masks used in two or more above-mentioned exposure processes.

[0022]In this invention, typically, the 1st alignment mark is formed in a support region around each field of two or more fields, and the 2nd alignment mark is formed in a support region of the outside of two or more fields. Typically, the 1st alignment mark and 2nd alignment mark have mutually different shape. Masks may be any of a transmission type mask and a stencil mask. In a transmission type mask, the 1st alignment mark and 2nd alignment mark are

formed by removing selectively electronic scatterer which the 1st alignment mark and 2nd alignment mark were formed in electronic scatterer formed on a membrane, and was especially formed on a membrane. In a stencil mask, the 1st alignment mark and 2nd alignment mark are formed in a mask substrate, By removing a mask substrate selectively especially, the 1st alignment mark and 2nd alignment mark are formed, and further from a viewpoint which aims at improvement in mark detection accuracy. The 1st alignment mark and 2nd alignment mark are formed by embedding metal which consists of an atom which has an atomic weight heavier than an atom which constitutes this mask substrate in a hole or a slot suitably formed by removing a mask substrate selectively. As such metal, platinum, gold, silver, copper, tungsten, tantalum, molybdenum, etc. can be used.

[0023]Exposure for forming the 1st alignment mark and 2nd alignment mark collectively, For example, it can carry out using actual size or a stepper exposure device of low reducing magnification, actual size or a scanner exposure device of low reducing magnification, a contact method one-shot exposure device, a proximity method one-shot exposure device, a mirror projection method one-shot exposure device, etc.

[0024]Suitably, size of a charged particle beam is 10 micrometers or less, and a charged particle beam exposure device with larger maximum deflection width of a charged particle beam without stage movement than the sum total of width of each field of two or more fields and width of a support region is used for exposure of a mask circuit pattern. After exposing a mask circuit pattern by a charged particle beam, formation of a mask circuit pattern is performed through development of resist, and subsequent etching, but. Before etching, it is desirable to cover the 1st alignment mark and 2nd alignment mark by a protective film, and for these marks to receive damage by an etching process, or to make it not destroyed.

[0025]In this invention constituted as mentioned above, By performing exposure for forming the 1st alignment mark in a support region of a member for mask production by package transfer, and forming a mask circuit pattern on the basis of this 1st alignment mark, Accuracy of position of the whole mask circuit pattern by this 1st alignment mark can be made very high. And even if distance between this 1st alignment mark changes a mask, it does not change. for this reason, a mask circuit pattern which forms a mask exposure machine for exposure for forming a mask circuit pattern in a small region -- a standard [alignment mark / 1st] -- accuracy -- good -- it can even expose -- what is necessary is just to carry out, and it is not necessary to use a mask exposure machine for expensive light beam exposure of a low throughput

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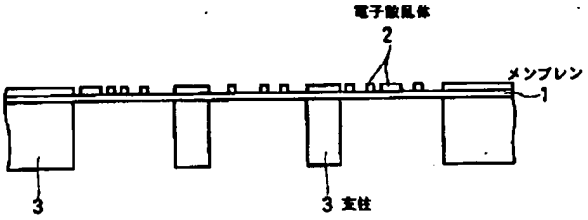
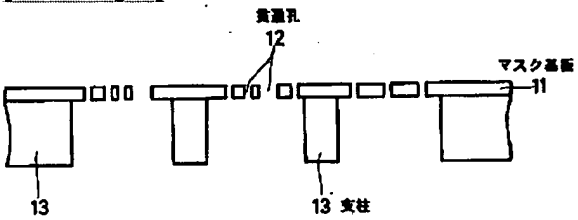
DRAWINGS

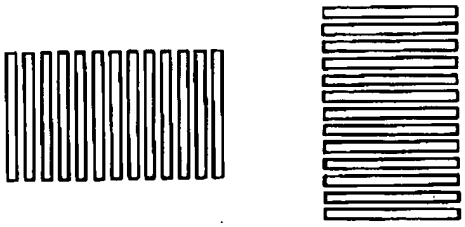
[Drawing 1]



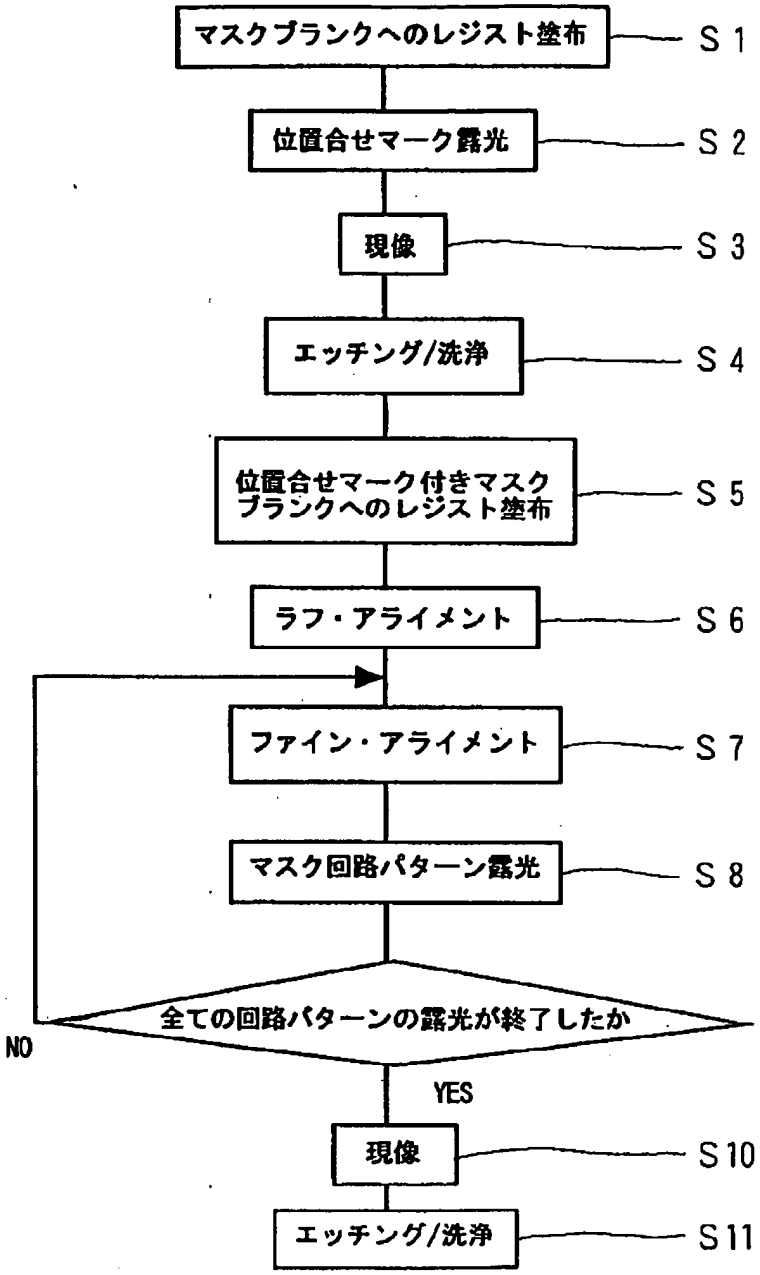
[Drawing 2]



[Drawing 6]

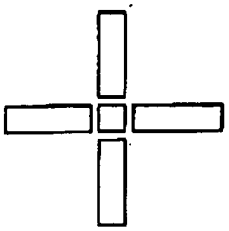


[Drawing 3]


マスクブランクへのレジスト塗布
S 1
位置合せマーク露光
S 2
現像
S 3
エッチング/洗浄
S 4
位置合せマーク付きマスクブランクへのレジスト塗布
S 5
ラフ・アライメント
S 6
ファイン・アライメント
S 7
マスク回路パターン露光
S 8
全ての回路パターンの露光が終了したか
NO
YES
現像
S 10
エッチング/洗浄
S 11

[Drawing 5]

A



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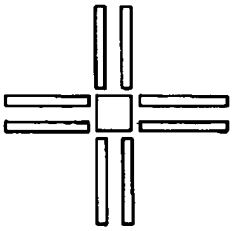

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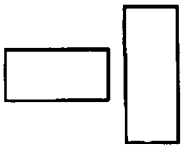

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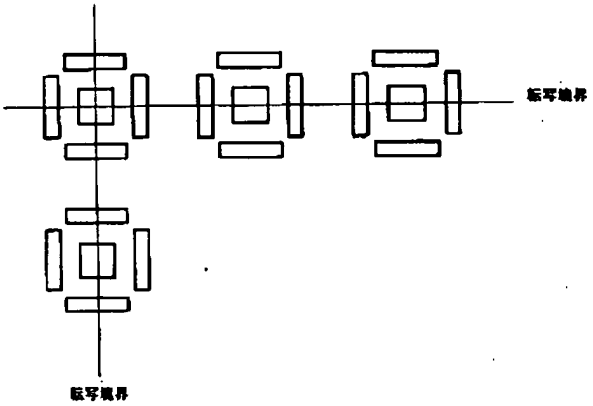

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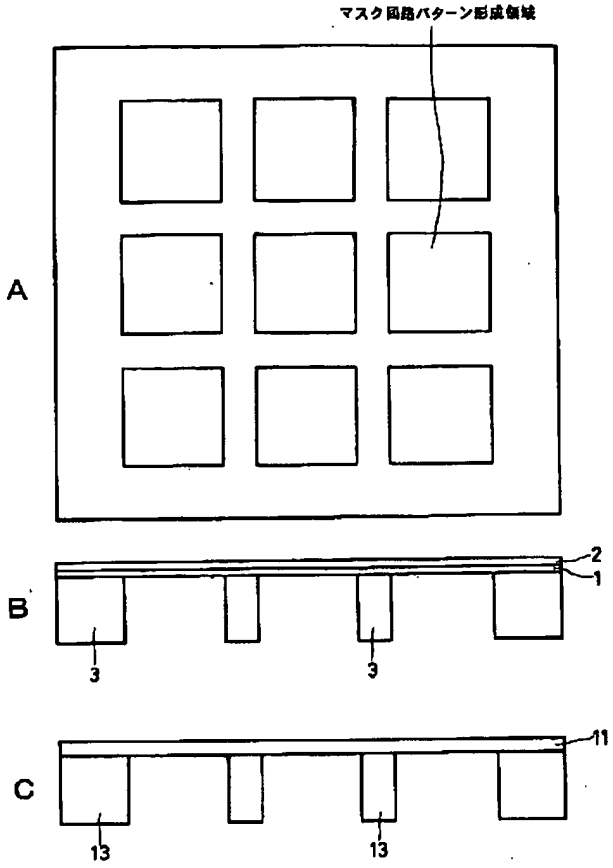

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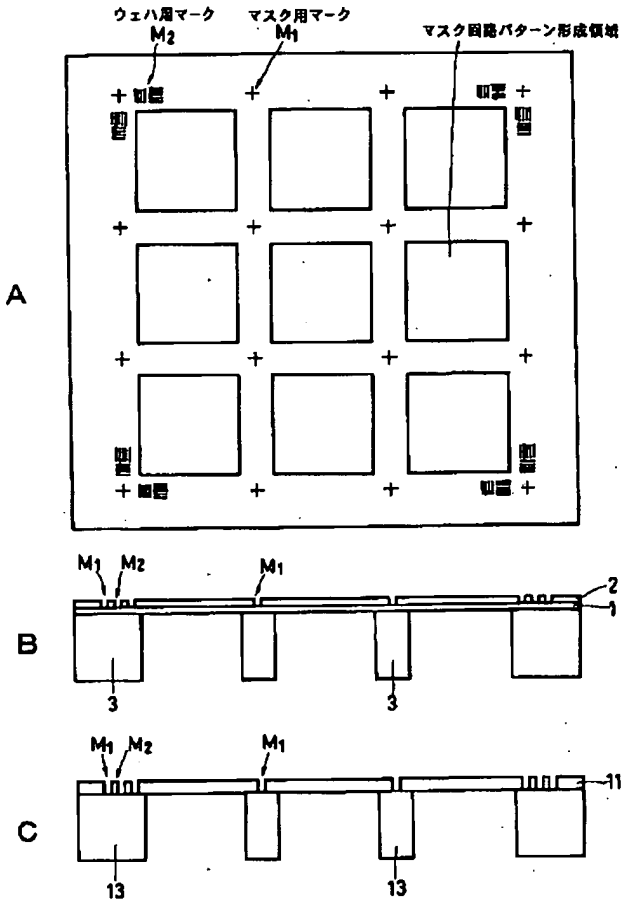
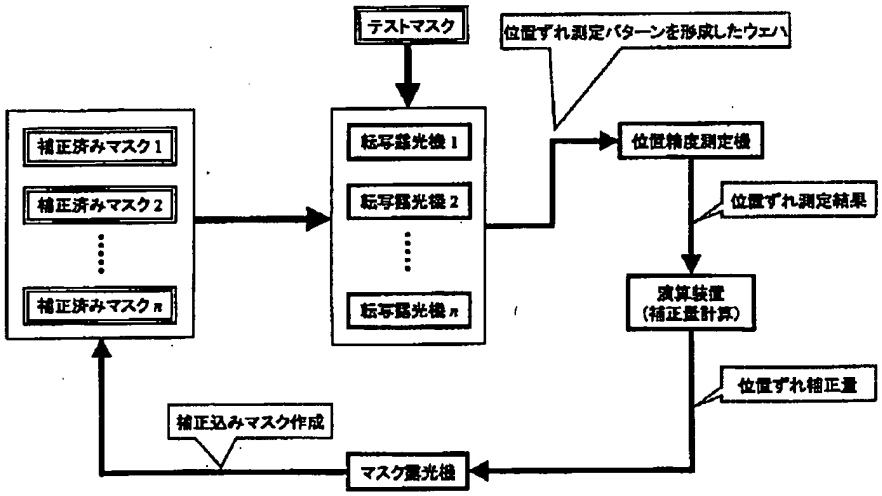
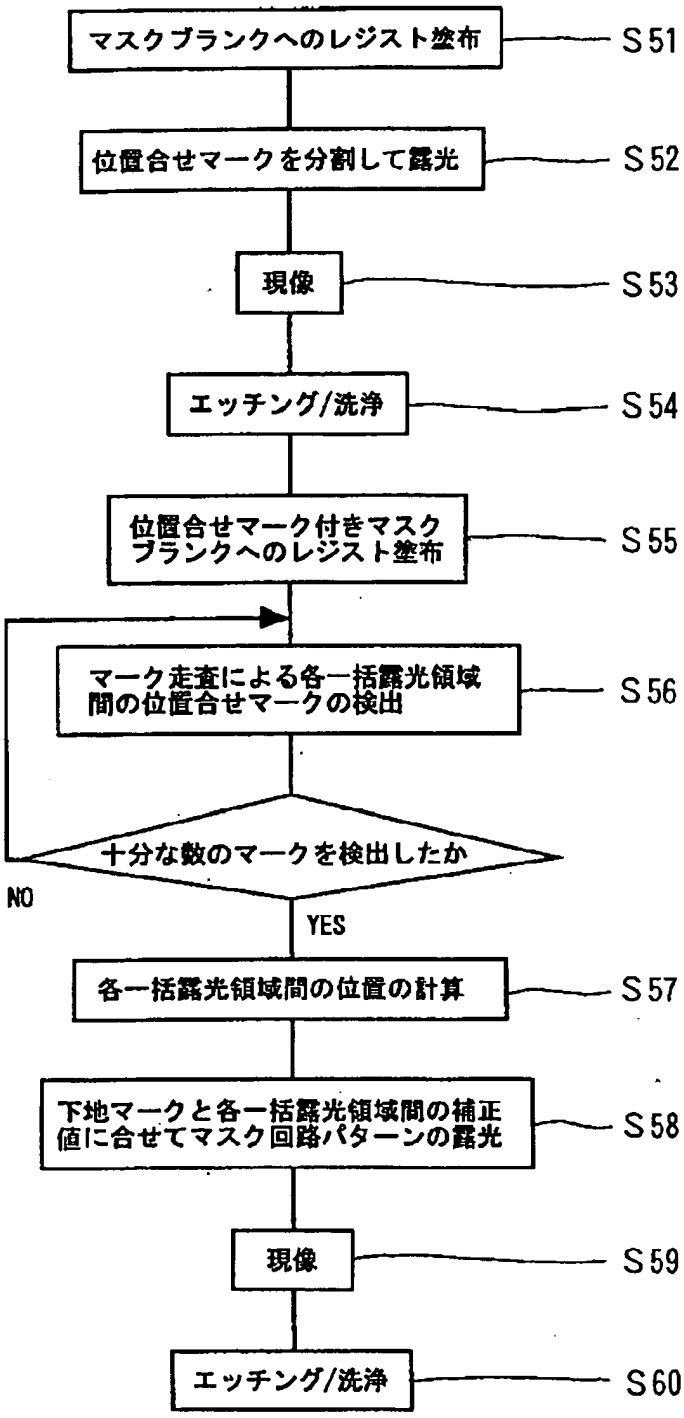


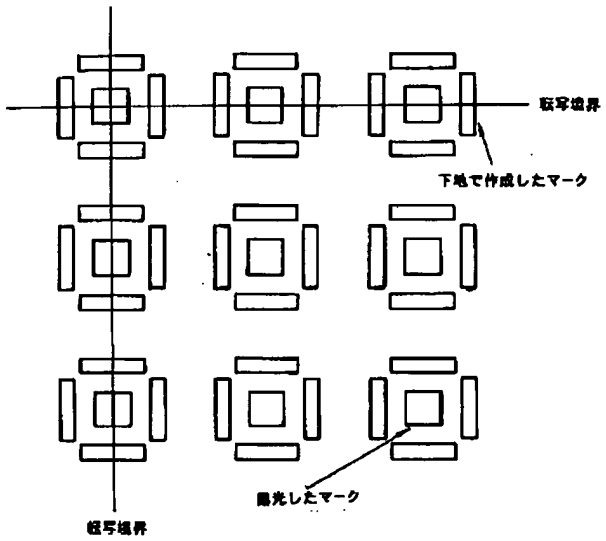
[Drawing 9]



[Drawing 8]


マスクブランクへのレジスト塗布
S51
位置合せマークを分割して露光
S52
現像
S53
エッチング/洗浄
S54
位置合せマーク付きマスクブランクへのレジスト塗布
S55
マーク走査による各一括露光領域間の位置合せマークの検出
S56
十分な数のマークを検出したか
NO
YES
各一括露光領域間の位置の計算
S57
下地マークと各一括露光領域間の補正値に合せてマスク回路パターンの露光
S58
現像
S59
エッチング/洗浄
S60

[Drawing 13]



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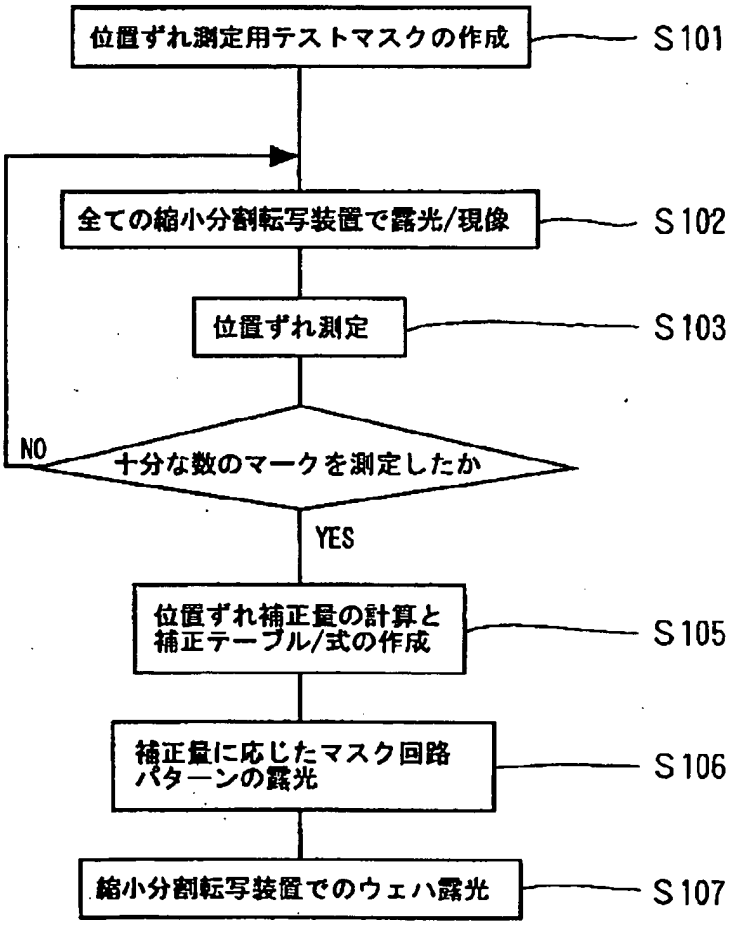
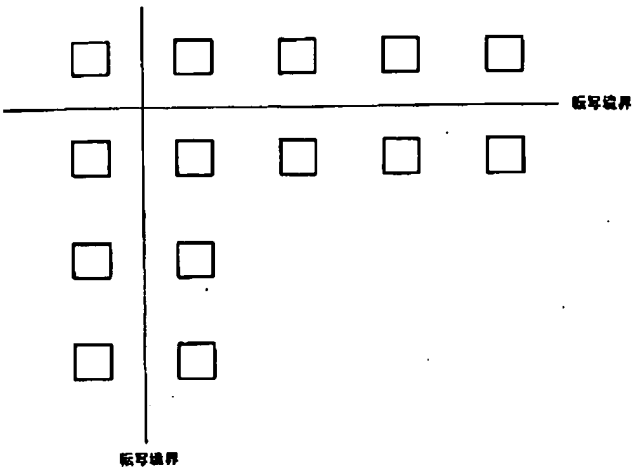


[Drawing 11]



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